# METHOD AND APPARATUS FOR DETECTING ARRAY DEGRADATION AND LOGIC DEGRADATION

Abstract of the Disclosure

A method and apparatus are provided for detecting degradation, such as, array degradation and logic degradation, in integrated circuits (ICs) including, for example, application specific integrated circuits (ASICs). A monitor built-in self-test (MBIST) engine is provided. At least one monitor element is coupled to the MBIST engine and is defined by predefined circuit elements in the integrated circuit. The MBIST engine is used for controlling operation of at least one monitor element for communicating with monitor bits to identify degradation of signal, timing and voltage margins.